IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a transistor formed on the semiconductor substrate, and having a gate electrode and first and second diffusion layers;

a first insulating film formed on the transistor;

a first multi-layer interconnect layer formed in the first insulating film, and including a plurality of interconnect layers and contacts;

a first recessed portion formed to continuously and vertically penetrate the first insulating film including at least two layers of the first multi-layer interconnect layer, and arranged so that at least part of the first recessed portion overlaps with the gate electrode; and

a ferroelectric capacitor three-dimensionally formed in the first recessed portion, and having first and second electrodes and a ferroelectric film, the first electrode being electrically connected with the first diffusion layer,

the ferroelectric capacitor comprising a first portion which is formed at a bottom of the first recessed portion and is extended horizontal to the semiconductor substrate, and a second portion which is formed on a side wall of the first recessed portion and is extended vertical to the semiconductor substrate.

2. (Original) The device according to claim 1, wherein the first electrode is electrically connected with the first diffusion layer via the first multi-layer interconnect layer.

3. (Original) The device according to claim 1, further comprising:

a second multi-layer interconnect layer formed in the first insulating film, electrically connected with the second diffusion layer, and including a plurality of interconnect layers and contacts; and

a bit line electrically connected with the second multi-layer interconnect layer, and arranged above the ferroelectric capacitor.

4. (Original) The device according to claim 1, wherein an aspect ratio of the first recessed portion is 1.

5. (Original) The device according to claim 1, wherein an aspect ratio of the first recessed portion is 4 to 5.

6. (Currently Amended) The device according to claim 1, wherein a peripheral circuit section arranged on the periphery of a memory cell section which includes the transistor and the ferroelectric capacitor, the peripheral circuit section comprises a second multi-layer interconnect layer formed on a surface identical to the first multi-layer interconnect layer in the first insulating film, and including a plurality of interconnect layers and contacts.

7. (Original) The device according to claim 1, further comprising:

a second insulating film formed under a bottom surface of the first recessed portion, and having at least one of stopper, hydrogen barrier and oxygen barrier functions.

8. (Original) The device according to claim 1, further comprising:

a first contact electrically connected with the second diffusion layer; and

a bit line electrically connected with the first contact, and arranged below the ferroelectric capacitor.

9. (Original) The device according to claim 1, further comprising:

a single- or plural-layer hydrogen barrier film formed to coat at least part of the side, bottom and upper surfaces of the ferroelectric capacitor.

10. (Original) The device according to claim 9, wherein the hydrogen barrier film has a first part formed at the side and bottom surfaces of the ferroelectric capacitor, and a second part formed on the upper surfaces of the ferroelectric capacitor,

the first part is formed of a conductive or insulating material, and the second part is formed of an insulating film.

11. (Original) The device according to claim 1, further comprising:

a single- or plural-layer oxygen barrier film continuously formed under the first electrode in the first recessed portion and on the first insulating film.

12. (Original) The device according to claim 1, further comprising:

a single- or plural-layer oxygen barrier film formed on the side and bottom surfaces of the first recessed portion and on the first insulating film; and

a single- or plural-layer hydrogen barrier film formed between the oxygen barrier film and the first electrode and formed to coat at least part of an upper surface of the ferroelectric capacitor.

13. (Original) The device according to claim 1, wherein the first electrode contacts

with an uppermost-layer interconnect of the first multi-layer interconnect layer via a single- or plural-layer reaction preventing conductive film.

14. (Original) The device according to claim 13, wherein a contact surface of the uppermost-layer interconnect and the first electrode is a flat or concavo-concave surface.

15. (Original) The device according to claim 1, further comprising:

a first contact formed on the first diffusion layer and under the ferroelectric capacitor, and electrically connected with the first diffusion layer and the first electrode.

16. (Original) The device according to claim 1, wherein a contact formed of part of the first electrode is electrically connected with the first diffusion layer.

17. (Original) The device according to claim 1, wherein a contact formed of part of the first electrode is electrically connected with the first diffusion layer via a single- or plural-layer reaction preventing conductive film.

18. (Original) The device according to claim 1, further comprising:

a single- or plural-layer oxygen barrier film formed on at least side and bottom surfaces of the first recessed portion;

a single- or plural-layer hydrogen barrier film formed between the oxygen barrier film and the first electrode and formed to coat at least part of an upper surface of the ferroelectric capacitor;

a first contact formed on the first diffusion layer and under the ferroelectric capacitor, and electrically connected with the first diffusion layer and the oxygen barrier film.

19. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a first transistor formed on the semiconductor substrate, and having a first gate electrode, first and second diffusion layers;

a second transistor formed on the semiconductor substrate, and having a second gate electrode, second and third diffusion layers;

a first insulating film formed on the first and second transistor;

first to third multi-layer interconnect layers formed in the first insulating film, and including a plurality of interconnect layers and contacts;

a first recessed portion formed to continuously and vertically penetrate the first insulating film including at least two layers of the first to third multi-layer interconnect layer, and arranged so that at least part of the first recessed portion overlaps with the first gate electrode;

a second recessed portion formed to continuously and vertically penetrate the first insulating film including at least two layers of the first to third multi-layer interconnect layer, and arranged so that at least part of the ~~first~~ second recessed portion overlaps with the second gate electrode;

a first ferroelectric capacitor three-dimensionally formed in the first recessed portion, and having first and second electrodes and a first ferroelectric film, the first electrode being electrically connected with the first diffusion layer via the first multi-layer interconnect layer, the first ferroelectric capacitor comprising a first portion which is formed at a bottom of the first recessed portion and is extended horizontal to the semiconductor substrate, and a second portion which is formed on a side of the first recessed portion and is extended vertical to the semiconductor substrate; and

a second ferroelectric capacitor three-dimensionally formed in the second recessed portion, and having third and fourth electrodes and a second ferroelectric film, the third electrode being electrically connected with the third diffusion layer via the third multi-layer interconnect layer, the second and fourth electrodes being electrically connected with the second diffusion layer via the second multi-layer interconnect layer, the second ferroelectric capacitor comprising a third portion which is formed at a bottom of the second recessed portion and is extended horizontal to the semiconductor substrate, and a fourth portion which is formed on a side of the second recessed portion and is extended vertical to the semiconductor substrate.

20. (Withdrawn) A method of manufacturing a semiconductor memory device, comprising:

forming a transistor having a gate electrode and first and second diffusion layers on a semiconductor substrate;

forming a first insulating film on the transistor;

forming a first multi-layer interconnect layer including a plurality of interconnect layers and contacts in the first insulating film;

forming a first recessed portion continuously and vertically penetrating the first insulating film including at least two layers of the first multi-layer interconnect layer at a position such that at least part of the first recessed portion overlaps with the gate electrode;

successively forming first electrode, ferroelectric film and second electrode in the first recessed portion; and

patterning the first electrode, ferroelectric film and second electrode to form a three-dimensional ferroelectric capacitor in the first recessed portion.

21. (New) The semiconductor memory device according to claim 1, wherein the first electrode is a bottom electrode, and the second electrode is a top electrode,

the semiconductor memory device further comprising:

a first contact formed above the ferroelectric capacitor and connected with the first electrode and the first multilayer interconnect layer; and

a second contact formed above the ferroelectric capacitor, connected with the second electrode, and being at a same level as the first contact.

22. (New) The semiconductor memory device according to claim 19, wherein the first electrode and the third electrode are bottom electrodes, and the second electrode and the fourth electrode are top electrodes,

the semiconductor memory device further comprising:

a first contact formed above the first ferroelectric capacitor and connected with the first electrode and the first multilayer interconnect layer;

a second contact formed above the first ferroelectric capacitor, connected with the second electrode, and being at a same level as the first contact;

a third contact formed above the second ferroelectric capacitor, connected with the third electrode and the second multi-layer interconnect layer, and being at a same level as the first contact; and

a fourth contact formed above the first ferroelectric capacitor, connected with the fourth electrode, and being at a same level as the first contact.